IN THE ABSTRACT

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ABSTRACT

A technique and circuit is provided for facilitating a faster settling time for a digital filter for use with an analog-to-digital converter. An exemplary technique utilizes a composite filter for a faster settling, lower noise resolution filter in a parallel configuration with a slower settling, higher noise resolution filter. As a result, valid data can be received faster for processing by the analog-to-digital converter. In addition, a composite digital filter circuit can include a three filter configuration including a fast-settling, low resolution first filter, a slower-settling, higher resolution second filter, and an even slower-settling, even higher resolution third filter, each of the filters configured in a parallel arrangement. Additional or fewer filters can also be provided. Moreover, the gain of each filter path can be suitably matched to the gain of any other filter path in the digital filter circuit to provide a filter output having an equalized gain regardless of the filter path selected. For example, a filter path can be suitably configured with a multiplier component such that an equalized gain can be realized for each filter path. In addition, the various filters of the digital filter circuit can be configured within the parallel arrangement to provide reduce layout requirements through the sharing of components. For example, a second filter can share at least two integrators with the third filter, and the first filter can share at least one integrator with the third filter. Further, the digital filter can be suitably configured for operation in various industrial applications. For example, the first filter can be suitably configured with a notch filter configured to replace the first, third and other odd harmonic notches of the first filter.